TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT (Under 37 CFR 1.97(b) or 1.97(c))	Docket No. BUR920030135US1

In Re Application Of: **Allen et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
10/709292	04/27/2004	**Unassigned**	**Unassigned**

Title: **INTEGRATED CIRCUIT YIELD ENHANCEMENT USING VORONOI DIAGRAMS**

Address to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

37 CFR 1.97(b)

1. ☒ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

37 CFR 1.97(c)

2. ☐ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:

   ☐ the statement specified in 37 CFR 1.97(e);

   OR

   ☐ the fee set forth in 37 CFR 1.17(p).

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INTEGRATED CIRCUIT YIELD ENHANCEMENT USING VORONOI DIAGRAMS

Payment of Fee

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

☐ A check in the amount of is attached.

☒ The Director is hereby authorized to charge and credit Deposit Account No. **090456** as described below.

- ☐ Charge the amount of
- ☒ Credit any overpayment.
- ☒ Charge any additional fee required.

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Signature of Person Mailing Correspondence

C. MUELLER

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***This certificate may only be used if paying by deposit account.**

Richard Kotulak

Signature

Dated: May 19, 2004

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cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

Allen et al.

Serial No.: ~~Not Yet Assigned~~ 10/709,292 Group Art Unit: Unknown

Filing Date: ~~Concurrently Herewith~~ 04/27/04 Examiner: Unknown

For: INTEGRATED CIRCUIT YIELD ENHANCEMENT USING VORONOI DIAGRAMS

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicants' duty of disclosure under 37 CFR §1.56, applicants respectfully bring the following documents, listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. Copies of the listed documents are provided herewith for the convenience of the Examiner. This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicants are aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456.

Respectfully submitted,

Frederick W. Gibb, III
Registration No. 37,629

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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
BUR920030135US1	10/709292 ~~Not Yet Assigned~~
Applicant(s) Allen et al.	
Filing Date 04/27/04 ~~Concurrently Herewith~~	**Group Art Unit** Unknown

*EXAMINER INITIAL	OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*
	Papadopoulou, E. and Lee, D.T., "Critical area computation via Voronoi diagrams," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Vol. 18, No. 4, pp .463-474, April 1999.
	Papadopoulou, E., "Critical area computation for missing material defects in VLSI circuits ," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Vol. 20, No. 5, pp 583-597, May 2001.
	Fook-Luen Heng and Zhan Chen. "VLSI Yield Enhancement Techniques Through Layout Modification." IBM T. J. Watson Research Center, pp. 1-15, July 17, 2000.
	A. Venkataraman and I. Koren. "Trade-offs between Yield and Reliability Enhancement." Proc. of the 1996 IEEE National Symposium on Defect and Fault Tolerance in VLSI Systems, pp. 67-75, November 1996.

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.